In the Drawings

FIGs. 1A and 1B are amended herein by adding the designation of "Prior Art" to the figure labels.

Attachments

Replacement Sheet

REMARKS

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, has tentatively rejected all claims. In response, Applicant submits the foregoing amendments and the following remarks.

Drawings Objections

A replacement sheet is provided herewith to provide replacement figures for Figures 1A and 1B. These replacement figures include the designation of "Prior Art," indicating that only that which is old is illustrated.

35 U.S.C 112 Rejections

The Office Action indicated that the specification is replete with terms, which are not clear. Applicant has reviewed the specification and, except for the minor typos or cosmetic corrections made herein, believes the specification to be in good and proper condition.

a. Page 1 in the specification

With regard to the objection noted in the Office Action regarding the description on page 1, Applicant notes that the test circuit and method of the application are used to determine whether the connections of chips on a circuit board are normal or not. The chip on a circuit board can be a FPGA chip. The FPGA chip (for example, Fig. 3a 31) connects with the circuit board by the pins of the FPGA chip and communicates with other chips by the BUS (for example, Fig. 3a 34) on the circuit board. By the use of the

test circuit and method of the application, determining whether the connections of chips on a circuit board are normal or not.

b. About the clarity of page 2 in the specification

With regard to the objection noted in the Office Action regarding the description on page 2, Applicant provides the following comments: First, clarifying the question about how a pattern is input to the shift register: A person skilled in the art will realize that a pattern indicates a digital signal composed of a series of 0/1 (for example, page 5, line 6, "01010001"), wherein 0 and 1 represent by corresponding voltage (for example, -5V for 0 and 5V for 1). The digital signal is input to the shift register in the form of voltage with a specific clock rate.

Second, clarifying the question about how a shift register of D-type flip-flops would 'process' a pattern, the shift registers of D-type flip-flops of the application are connected with a particular form. That is the conventional linear feedback shift register (page 2, line 3-4, etc.). There exists a certain relation between the input and output of the linear feedback shift register, (for example, $G(x)=\frac{\sum_{i=1}^{n} g_i x^i \left(a_{-i} x^{-i}+\cdots+a_{-1} x^{-1}\right)}{g(x)}$, page 5, line 17). The D-type flip-flops connected in this way do process the pattern rather shift the pattern out.

Third, clarifying the question about how an output pin would 'produce a specific pattern' and why a shift register would have an output pin. The specific pattern is a pattern produced by the above illustrated. The output pin producing "a specific pattern" herein indicates that the output pin outputs "a specific pattern". Otherwise, a

shift register and circuit elements communicating with other circuit elements by wire all have output pins to communicate with other circuit elements on the circuit board.

c. Claim Rejections

Turning now to the claim rejections: claim 1-13 stand rejected under 35 U.S.C. 112, as allegedly failing to comply with the enablement requirement (as well as 112, second paragraph, as allegedly indefinite). Applicant respectfully requests reconsideration of the rejections for at least the following reasons.

The supporting reasons for the rejections under 35 U.S.C. 112 of claim 1-13 appears to be similar to the reasons (discussed above) for the objections to the specification. Thus, for the reasons submitted above, Applicant submits that persons skilled in the art will have an enabled understanding of the claimed embodiments. For example, the Office Action states that it is unclear how a pattern is input to the shift register. However, as set forth above, a pattern indicates a digital signal composed of a series of 0/1 (for example, page 5, line 6, "01010001"), wherein 0 and 1 represent by corresponding voltage (for example, -5V for 0 and 5V for 1). The digital signal is input to the shift register in the form of voltage with a specific clock rate.

Thus, for at least the forgoing reasons, the rejections under 35 U.S.C. § 112 should be withdrawn.

Rejections Under 35 U.S.C 102

Claims 1 and 8 stand rejected under 35 U.S.C 102(e) as allegedly anticipated by Wang et al. U.S. Pre Grant publication 2002/0078412 (hereinafter the '412 application).

Applicant respectfully requests reconsideration of the rejections for at least the reasons hereinafter.

Regarding claim 1, the '412 application fails to disclose at least the claimed features of "disposing a first connection circuit on the first programmable array circuit according to a preset linear feedback shift register (LFSR) polynomial; disposing a second connection circuit on the second programmable array circuit according to the preset LFSR polynomial,……; and examining the particular pattern to acquire a connection status of the first and the second connection circuits." as expressly recited in the claim 1.

The embodiments of the present application connect the first and second programmable array circuits according to the preset LFSR polynomial and determines whether the connection between the first and second programmable array circuits is normal by comparing the relation between input and output signals and the relation built by the preset LFSR polynomial. The '412 application (in paragraphs 0009) describes operating plurality of programmable circuits having the same function with the clock and the reset signal and comparing the output of each programmable circuit to determine whether circuits are normal or not. The application determines the connection state between two programmable circuits. However, the '412 application determines the function of each programmable circuit. The LFSR circuit used in the '412 application (in paragraph 0011) is simply for simplifying a signature to a single word in order to reduce a comparing operation. However, the LSFR polynomial used in the present application is used to build a special relation between two programmable circuits in order to test the connection state. Accordingly, not only is the structure and operation of the

embodiments of claim 1 different that that of the '412 application, but the result is different as well.

For at least the forgoing reasons, independent claim 1 patently defines over the cited reference, and the rejection of claim 1 should be withdrawn. As claims 2-7 depend from claim 1, they patently define over the cited art for at least the same reasons.

Independent claim 8 defines over the cited art for similar reasons. Specifically, the '412 application fails to disclose at least the following features: "the first and the second connection circuits are disposed according to a preset linear feedback shift register (LFSR) polynomial, wherein a test pattern is input to and processed by the shift register, and then a particular pattern is produced from the shift register, and wherein the particular pattern is examined to acquire a connection status of the first and the second connection circuits," as expressly recited in claim 8.

As noted above in connection with claim 1, the embodiments of the present application determine the connection state between two programmable circuits. However, the patent '412 determines the function of each programmable circuits. For reasons discussed above in connection with claim 1, claim 8 similarly defines over the cited '412 application. As claims 9-13 depend from claim 8, they patently define over the cited art for at least the same reasons.

Conclusion

For the reasons as described above, all pending claims patently define over the cited art of record. If the Examiner believes that a telephone conference would expedite

the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

By: _____

Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500